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10/792,350	03/02/2004	Michael W. Leddige	5038-356	4528

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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	**PAPER NUMBER**
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/792,350	LEDDIGE ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/20/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is in response to application 10/792,350, amendment filed 2/20/2007. Claims 1-8 and 17-28 are currently pending in this application. Claims 1 and 5 are currently amended. Claims 17-28 are new.

Claim Objections

1. Claim 2 is objected to for the following reason(s): the recited language "nearside" and "far-side" are not defined in the specification and are indefinite. With respect to "nearside", the meaning of "a nearside column" in unclear in light of the specification. With respect to "far-side", the meaning of "a far-side column" is unclear in light of the specification. More specifically, the specification fails to clearly describe what is considered near or far with respect to the structure of the memory module being claimed. Examiner suggests amending claim 2 to clarify said recited language.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-8, 17-23 and 25-28 are rejected under 35 U.S.C. 102(e)** as being anticipated by Dickmann (US PG Pub 2004/0230932).

4. With respect to claim 1, Dickmann teaches:

an array of connections arranged in rows (i.e. row arrangements, paragraph [0036]) and columns (see Figure 2, memory module arrangement wired in an array of rows and columns) such that there are first and second outer columns (outer columns M1 and M4, paragraph [0036]), the connections (modules M1-M4 has connecting lines, paragraph [0038]) corresponding to electrical signals (individual signal lines corresponding to connections on the memory modules, paragraph [0075]), and those connections in the first and second outer columns (**selected** chips can be the two outer modules M1 and M4, see paragraph [0020]) can be interchanged (data interchange is performed between the **selected** group of semiconductor chips, paragraph [0014]) such that at least one of the electrical signals previously corresponding to at least one of the connections in the first outer column corresponds to at least one of the connections in the second outer column and at least one of the electrical signals previously corresponding to at least one of the connections in the second outer column corresponds to at least one of the connections in the first outer column (resulting in data lines being interchangeable as described in Applicant's specification on page 4, lines 15-25; then see Dickmann, Abstract, data interchange is performed between data lines DQ1-DQ72 in the data bus and the selected [i.e. outer columns M1 and M4] group of semiconductor chips).

5. With respect to claims 5 and 20, Dickmann teaches:

a first memory module (see memory modules of Figure 1) mounted on a first side of a substrate (dual-sided substrate with M1-M4 illustrated on one side, see paragraph [0038]) the first module comprising:

an array of connections arranged in rows (i.e. row arrangements, paragraph [0036]) and columns (see Figure 2, memory module arrangement wired in an array of rows and columns) such that there are first and second outer columns (outer columns M1 and M4, paragraph [0036]), the connections (modules M1-M4 has connecting lines, paragraph [0038]) corresponding to electrical signals (individual signal lines corresponding to connections on the memory modules, paragraph [0075]), and those connections in the first and second outer columns (**selected** chips can be the two outer modules M1 and M4, see paragraph [0020]) can be interchanged (data interchange is performed between the **selected** group of semiconductor chips, paragraph [0014]) such that at least one of the electrical signals previously corresponding to at least one of the connections in the first outer column corresponds to at least one of the connections in the second outer column and at least one of the electrical signals previously corresponding to at least one of the connections in the second outer column corresponds to at least one of the connections in the first outer column (resulting in data lines being interchangeable as described in Applicant's specification on page 4, lines 15-25; then see Dickmann, Abstract, data interchange is performed between data lines DQ1-DQ72 in the data bus and the selected [i.e. outer columns M1 and M4] group of semiconductor chips);

a second memory module mounted on a second side (DIMM dual sided memory wherein only one side of the modules M1-M4 are shown for purposes of clarity, see paragraph [0038], suggesting that an identical memory structure M1-M4 can exist on

the other side) of the substrate comprising the same structure as said first memory module (see above prior-art citations);

a memory controller (memory controller, paragraph [0006]) to control interchange (controlling the data interchange, paragraph [0006]) of signals between first and second outer columns (selected modules, i.e. M1 and M4 outer modules, see paragraph [0020]) of the memory modules; and

signal traces in the substrate, wherein the connection in the first and second outer columns of the first and second memory modules are arranged such that signals routed on the traces have uniform routing lengths (Figure 2 suggests that wiring of equal length exists connecting memory modules M1-M4 between chips and the controller C).

6. With respect to claim 2, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches: wherein the first outer column is a nearside column (see Fig 3, outer column M4 is nearest to memory controller C) and the second outer column is far-side column (see Fig 3, outer column M1 is farthest from the memory controller C).

7. With respect to claim 3, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches: wherein there are third and fourth outer columns having interchangeable connections (i.e. interchange is performed between the semiconductor chips in the selected group, wherein paragraphs [0018-0020] suggest that the selected group comprise the modules [i.e. columns]) M1 and M4, or M2 and M3, or another combination, see paragraphs [0014], [0018], and [0020]).

8. With respect to claims 4 and 8, Dickmann teaches all the elements of claims 1 and 5, from which the claims depend respectively. Dickmann teaches: the memory module further comprising a package selected from the group comprised of: X16, and X4/X8 (x4, see paragraph [0041]).

9. With respect to claim 6, Dickmann teaches all the elements of claim 5, from which the claim depends. Dickmann teaches: the substrate further comprising a multi-layered printed circuit board (i.e. memory modules plugged into a motherboard, paragraph [0034]).

10. With respect to claim 7, Dickmann teaches all the elements of claim 6, from which the claim depends. Dickmann teaches: signal traces further comprising multiple signal traces in multiple layers of the printed circuit board (i.e. discussion of the arrangement in a printed circuit board, paragraph [0036]).

11. With respect to claim 17, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches:

wherein the interchanged connections in the first and second outer columns comprise connections corresponding to address signals (see Abstract, data interchange occurs between data address lines DQ1-DQ72 with respect to the selected outer columns M1 and M4, see Abstract in conjunction with paragraphs [0014] and [0020]).

12. With respect to claim 18, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches: wherein the interchanged connections in

the first and second outer columns comprise connections corresponding to address signals (memory banks, Figures 4a and 4b).

13. With respect to claim 19, Dickmann teaches all the elements of claim 1, from which the claim depends. Dickmann teaches:

wherein the interchanged connections in the first and second outer columns comprise connections corresponding to data signals within a byte lane (see nine bit data buses, i.e. analogous to "byte-lane", see Figure 5).

14. With respect to claim 21, Dickmann teaches all the elements of claim 20, from which the claim depends. Dickmann teaches:

wherein the memory controller (memory controller, paragraph [0006]) interchanges (interchange, paragraph [0014]) a first signal previously corresponding to a first connection in the first column of the second memory module (dual sided memory module, paragraph [0038]) with a second signal previously corresponding to a second connection in the second column of the second memory.

15. With respect to claim 22, Dickmann teaches all the elements of claim 21, from which the claim depends. Dickmann teaches:

wherein the second memory module is mounted on a second side of the substrate (see discussion of dual-sided memory module, paragraph [0038]).

16. With respect to claim 23, Dickmann teaches all the elements of claim 22, from which the claim depends. Dickmann teaches:

wherein at least one of the signal traces in the substrate connects the second connection with a third connection in the first column of the first memory module

(interchange between DQ1 through DQ72, i.e. multiple connection interchanges in outer columns, see Abstract and paragraph [0020]).

17. With respect to claim 25, Dickmann teaches: wherein a length between a bus connection and the second connection is substantially uniform with a length between the bus connection and the third connection (see Figure 2, Figure 2 discloses this uniformity feature).

18. With respect to claim 26, Dickmann teaches all the elements of claim 21, from which the claim depends. Dickmann teaches:

wherein the first signal and the second signal are data signals with a byte lane (see Figure 5, 9 bit data bus analogous to 8-bit byte lane).

19. With respect to claim 27, Dickmann teaches all the elements of claim 20, from which the claim depends. Dickmann teaches:

wherein the second memory module is stacked on the first memory module (dual-sided memory module, see paragraph [0038]).

20. With respect to claim 28, Dickmann teaches all the elements of claim 20, from which the claim depends. Dickmann teaches:

wherein the second memory module further comprises a third and fourth outer columns (see Figure 5, see M2 and M3, which can be considered the third and fourth outer columns as the next set of outer columns next to M1 and M4).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claim 24 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Dickmann in view of Kozaru (2004/0012991).

23. With respect to claim 24, Dickmann fails to teach: at least one via completely penetrating the substrate, wherein the second connection is connected to the third connection through the via.

However, Kozaru teaches: at least one via completely penetrating the substrate, wherein the second connection is connected to the third connection through the via (wires connected through vias penetrating the module substrate, see Kozaru, paragraph [0074]).

It would have been obvious to one of ordinary skill in the art to incorporate Kozaru's use of vias into the invention of Dickmann for at least the following reason(s): paragraph [0074] of Kozaru suggests that one useful way to connect a front and rear surface mounted on the front and rear side of a substrate is to use via connections to make connections from one surface on one side of a substrate to the other surface on the other side of the substrate (see paragraph [0074] of Kozaru).

Response to Arguments

24. Applicant's arguments filed 2/20/2007 have been fully considered but they are not persuasive. The applicable prior-art rejections from the previous office action are incorporated herein.

25. Applicant asserts that: the data interchange described by Dickmann, for example, paragraph [0014], refers to the exchange of data between the chips and the system bus, not interchanging signals corresponding to columns of connections on a chip or module. Examiner disagrees with this assertion.

26. Examiner points out that the abstract of Dickmann discloses: data interchange is performed between the data lines (DQ1-DQ72) in the data bus, wherein DQ1-DQ72 are the addresses of the data lines corresponding to connections of the memory modules as described in paragraph [0041]. Further, paragraph [0014] discloses that data interchange is performed between semiconductor chips in the selected group, wherein the selected group can consist of the outer column modules M1 and M4 as described in paragraph [0020].

27. With respect to Applicant's arguments that Dickmann does not teach interchanging actual signals corresponding to columns of connections and only teaches performing a data interchange, Examiner points out that Applicant's specification fails to teach a method or apparatus wherein the signals of a memory module can be physically interchanged to connect at another location when the memory module is presumed to be already manufactured or processed. More specifically, Applicant's memory module, as described in the specification, is only capable of interchanging the data lines at different addresses such as DQ[0:7] and DQ[8:15] as described on page 4 lines 15-20. Therefore, Examiner points out that Dickmann teaches interchanging data on specific address lines corresponding to the outer columns of a memory module.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL DINH
PRIMARY EXAMINER

Suchin Parihar
Examiner
AU 2825